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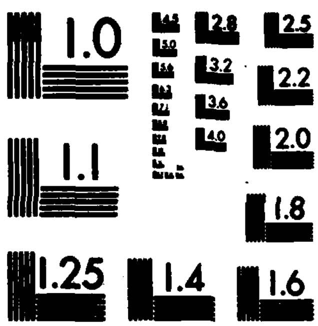

MICROCOPY RESOLUTION TEST CHART
NATIONAL BUREAU OF STANDARDS-1963-A

CONTRACT MDA 903-81-C-0389

Final Technical Report
Covering Activities from
September 1982 through April 1983

Prepared for
Defense Advanced Research Agency
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INTRODUCTION

Itek and Bell-Northern Research (BNR) have performed preliminary development of a 2048 x 96 element time delay and integrated (TDI) CCD Charge coupled devices which is buttable end to end with a gap of two pixels. The device has 13 ~~μm~~ micrometers pixels and is designed with several special features making it ideal for high quality reconnaissance imaging. The status at the beginning of this work was that a limited number of samples had been fabricated, validating the basic design, but some room for improvement had been recognized.

Separate contracts were thus granted to Itek and BNR for the purpose of furthering this development by the Defense Advanced Research Projects Agency. The purpose of this Final Report is to discuss the activities since the Mid Term Report.

OBJECTIVE

The objective of the work defined is to facilitate the further development of the E57 series CCDs through improvements in (a) CCD design techniques and (b) silicon wafer processing techniques. In each case, the intent is to validate the improvements through demonstration on smaller test wafers before committing to the change on the full 2048 x 96 element E57 CCDs.

TASKS DEFINITION

The following tasks were defined in support of the above objective:

Task 1 - Design Techniques

Design 512 x 96 CCD circuits incorporating a number of the design improvements which are proposed, but have not been validated. Except for

the intended changes, and the reduced extent, the design will be identical to the E57B. One circuit will be completely identical to the E57B. Incorporate these modified circuits along with test inserts into a test mask and fabricate the mask set. Fabricate wafers and test for results.

Task 2 - Processing Technology

Investigate several processing modifications intended to bring about improvements in dark current, MTF, speed, and manufacturing yield. In particular:

a) Characterize some on-hand wafers from a test mask set (E42) which had been fabricated with a number of processing variations to investigate improved gettering techniques.

b) Perform process modelling to incorporate proposed process variations into the SUPREM3 model.

c) Fabricate wafers with an existing test mask set, the W62, in order to investigate the potential benefits of dual dielectric (Si_3N_4 + SiO_2) and high pressure gate oxidation (HIPOX).

d) Investigate new electrode materials, particularly amorphous silicon, silicides, and polycides to see if improved electrical or optical properties might result.

PROGRESS

Progress on Tasks 1 and 2 was as follows.

Task 1

The design and mask procurement for a test chip with three 512 x 96 TDI imagers, designated the W66, were completed during the first portion of the contract period and reported on in the Mid Term Report. The overall layout of that chip is shown in Figure 1.

Wafer Fabrication. Two batches of 10 wafers each were processed on this contract. The first batch was probe tested and found to have been completely lost due to processing problems. All devices tested suffered from shorts between the first and second levels of metal, due to pinholes in what is normally only a scratch protection layer. Second level metal, requiring a high quality pinhole free dielectric isolation, is not a standard process at BNR, and apparently the pyrox scratch protection layer needs to be better controlled if it is to be used for that purpose.

The second batch was successfully processed with all wafers producing numerous working devices. Some processing variation was done to allow evaluation of variations in the amount of compensation implant and in the anneal cycle after implant. Five wafers were subjected to 100% probe testing to obtain yield information. For all five wafers, a functional yield (works completely, but not tested to a performance specification) of 75% to 80% was obtained. This serves as the basic verification of all three designs and of the fact that the design improvements were successful.

Based on the five wafer 100% probe and on testing of a smaller number of packaged chips at BNR and at Itek, the following comments may be made concerning the specific design improvements.

Bonding pads. The bonding pads were increased in size to 140 μm x 250 μm in order that the more extensive probe testing that these devices undergo at BNR and then at Itek may be performed without compromising the ability to bond to them.

Gate protection. Protection devices consisting of an RC network with a diode shunt were incorporated on a number of low capacitance gates that had been susceptible to electrostatic discharge (ESD) damage. An ESD tester which simulated electrical discharge from human handling showed that protected gates could handle about 550v discharges before being damaged while the unprotected ones were damaged with less than 100v. High frequency clocking at up to 8 MHz showed that no harmful effects on signal waveforms had been caused.

Clock feedthrough. Both the mid- and end- taps were redesigned to reduce several undesireable capacitive coupling phenomena which produce objectionable output waveforms. The mid-tap clock coupling was successfully reduced into the noise level while the end clock signal was significantly reduced to about 10 mv, 1% of the peak signal. Initial testing at BNR suggested that speed of response had been compromised, but subsequent testing at Itek with voltages optimized showed the redesigned taps to be at least as fast as those of the E57.

Fixed pattern noise. A particular electrode connection which produces a fixed pattern was redesigned to reduce the effect from about 20%

of the signal for the affected pixels to about 10%. A technique for further reduction was also identified for incorporation in the next generation of the E57 series.

Reset voltage. The reset transistor was changed from enhancement mode to depletion mode, reducing the required reset voltage from 25v to 15v.

E1 Mode Optical Window. The metal masking was altered so that the sensitivity in the E1 (single line sensor) mode would be closer to the nominal 1/96 of the sensitivity in the E96 (full TDI) mode that was intended.

Redesigned butt edge. The edges of the chip were redesigned in order to reduce the size of the achievable gap from four pixels to the goal of two pixels and at the same time reduce spurious charge accumulated in the extreme pixels. The complexity at the ends combined with the requirement for a continuous guard band resulted in some design rules being bent slightly. With the use of a DSW 4800 stepper and positive photoresist, the photolithographic fabrication was successful, as noted from the yield statistics above. The new technique was not completely evaluated, due to loss of Batch 1, which was to have included the chemical etching experiments. It was concluded, however, that the basic design works and is an improvement suitable for incorporation in the next generation of E57 with respect to both the gap and spurious charge.

Summary for Task 1

A number of improvements were designed, fabricated, and evaluated. In most cases, the original goals were met; in those cases where the goal

was not entirely met, the improvement was sufficient to incorporate the improvement in the next generation of E57. A redesign of the E57 based on these results is now in progress as part of an ongoing Itek IR&D program.

Task 2

Task 2 contained several sub tasks related to the optimization of some of the process parameters and the development of new process steps. Much of the laboratory work was completed during the first portion of the contract, and efforts since the Mid-Term Report have consisted mainly of analyzing the results and drawing conclusions.

Gettering characterization. Sixty-six wafers fabricated with controlled, matrixed variations in material supplier, gettering implant, and anneal cycle were analyzed for dark current and carrier lifetime. It was found that with proper choice of process and material, not greatly different from the previous processing, a level of dark current in the TDI devices of less than 0.5 na/cm^2 at the standard temperature of 20 degC is readily achievable in about 75% of the working devices.

Dual dielectric. One batch of W62 CCDs (a 512 x 96 TDI imager test mask set) was fabricated after SUPREM3 modelling and a dummy batch that only underwent the dielectric fabrication. The dual dielectric consisted of 400Å of CVD Si_3N_4 over 700Å of SiO_2, and required altering about 20% of the process sequence. A few wafers were also run as controls with all of the standard process steps. The yield for functional probe testing was over 50% for both process variations, indicating that the altered process was successful the first time. Sensitivity and saturation level were both about

40% higher for the dual dielectric version, a possible indication that amplifier gain was higher. Transfer efficiency was measured to be greater than 0.99997. The dark current was higher than usually found, about 4 na/cm^2 at 20 degC, but was also similarly high in the standard process single dielectric controls.

HIPOX. The use of oxides grown at high pressure was investigated in order to allow oxides to be grown at low temperature without the time required becoming unacceptable. Following SUPREM3 modelling, a process at 920 degC and 10 atm was defined. Some other process parameters such as implants were changed to account for the different temperature cycles. Some matrixing was done to investigate whether gate only or both gate and field oxides might be HIPOX. Results were somewhat similar to the dual dielectric experiment. High yield (about 80% functional) was obtained on the first run, indicating that with the modelling, the new process step was properly designed. Transfer efficiency was greater than 0.99995. Dark current was also found to be higher than usual at 2 to 3 na/cm^2 at 20 degC, but again the standard process controls were similarly high.

Electrode materials. Amporphous silicon (about 3900Å), four silicides (about 3000Å of $TaSi_2$, $TiSi_2$, $MoSi_2$, or WSi_2) and four polycides (about 750Å of the same four silicides on about 3000Å of poly) were prepared and measured for optical transmission and electrical resistivity. Standard poly was also prepared. There was some variation in deposition technique and temperature for the new materials. The amorphous silicon shows some promise in that it has slightly higher transmission than poly with about half the resistance and excellent uniformity. This indicates that an optimized amorphous

silicon conductor might have significantly higher transmission than poly, particularly in the 0.35 to 0.5 μm spectral band where front side illuminated imagers with polysilicon gates are deficient in sensitivity. The silicides generally appeared unuseable in that they were opaque when thick enough to be good conductors. The polycides showed some transmission at electrically useable thicknesses, and there is some chance that optimized layers of them might be useable.

Task 2 Summary

Several potential process variations and new process steps were evaluated for possible incorporation into the standard process in the future. Optimized gettering shows great promise for dark current reduction and will be used in the next generation of E57 imager. Dual dielectric and HYPOX process steps were both verified and may be considered as available for incorporation if needed. Some new gate electrode materials were investigated, and at least one, amorphous silicon, appears to show some promise, although further development is needed.

PROGRAM SUMMARY

Further development of the Itek/BNR E57 series of 2048 x 96 pixel TDI imaging CCD has been facilitated, thus increasing its availability to other government programs. Both design improvements and process improvements were developed and/or validated, thus allowing their incorporation into the next generation E57C design which is now under way at Itek and BNR on the ongoing Itek IR&D program.

W66A DESIGN

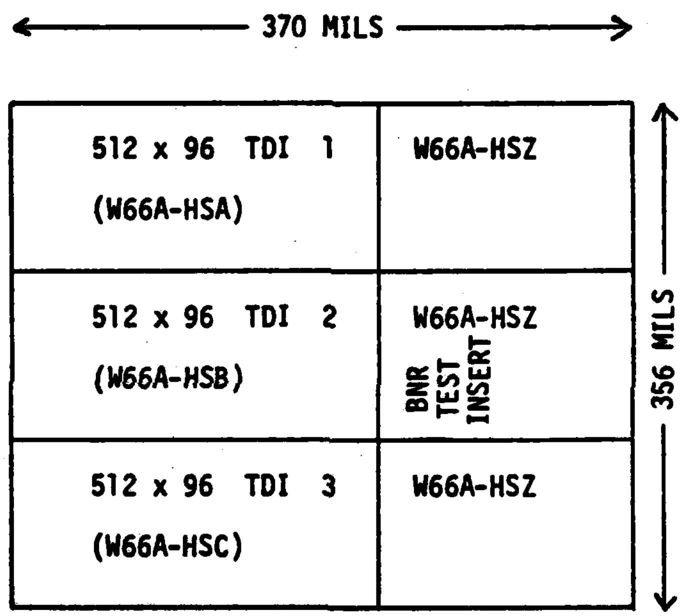

FIG. 1 ORGANIZATION OF W66A